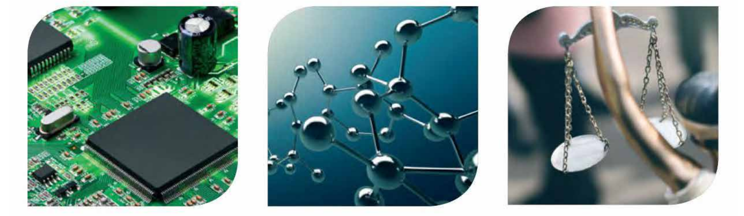
eurofins | EAG Laboratories



Enhanced Dye and Pull Analysis for CSP Package Types

By Sinai Galvan, Eurofins EAG Laboratories, Sunnyvale, CA, USA
www.eag.com

ABSTRACT

In this paper, we successfully demonstrate the feasibility of performing Dye and Pull (D&P) Analysis on Chip Scale Package (CSP) types, for which the lab previously experienced structural failure during the pulling process repeatedly which greatly limited the useful information obtained.

INTRODUCTION

Chip Scale Packages (CSP) are widely used in modern electronics and ensuring their performance are critical. While standard Dye and Pull testing is a well-established method for assessing the integrity of Ball Grid Arrays (BGA's), its direct application to CSP's presents challenges. These enhanced methodologies customized to CSP's offers an approach for CSP testing which benefits industries focused on high-performance and small electronics.

EXPERIMENTAL & RESULTS

Standard Dye and Pull Analysis for CSP Package Types:

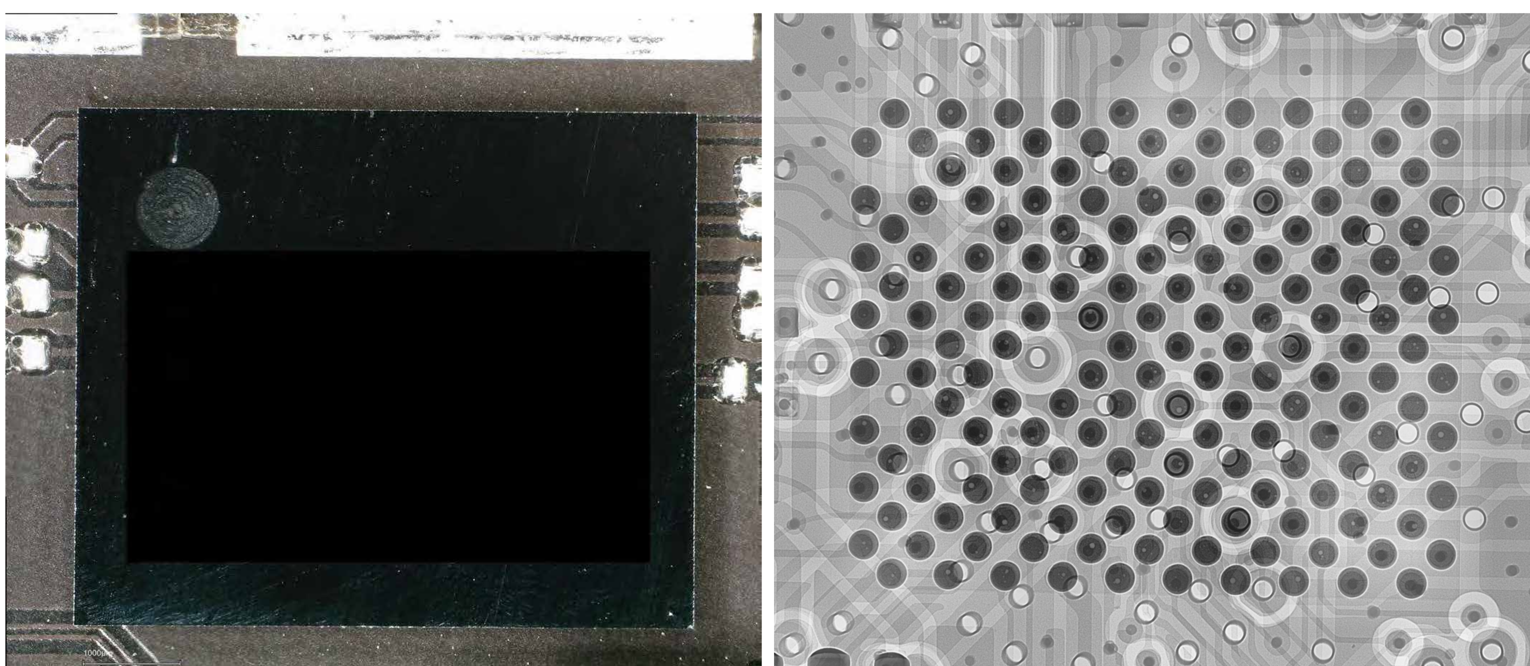


Figure 1: Enhanced Dye & Pull process used to improve success rates on CSP package types.

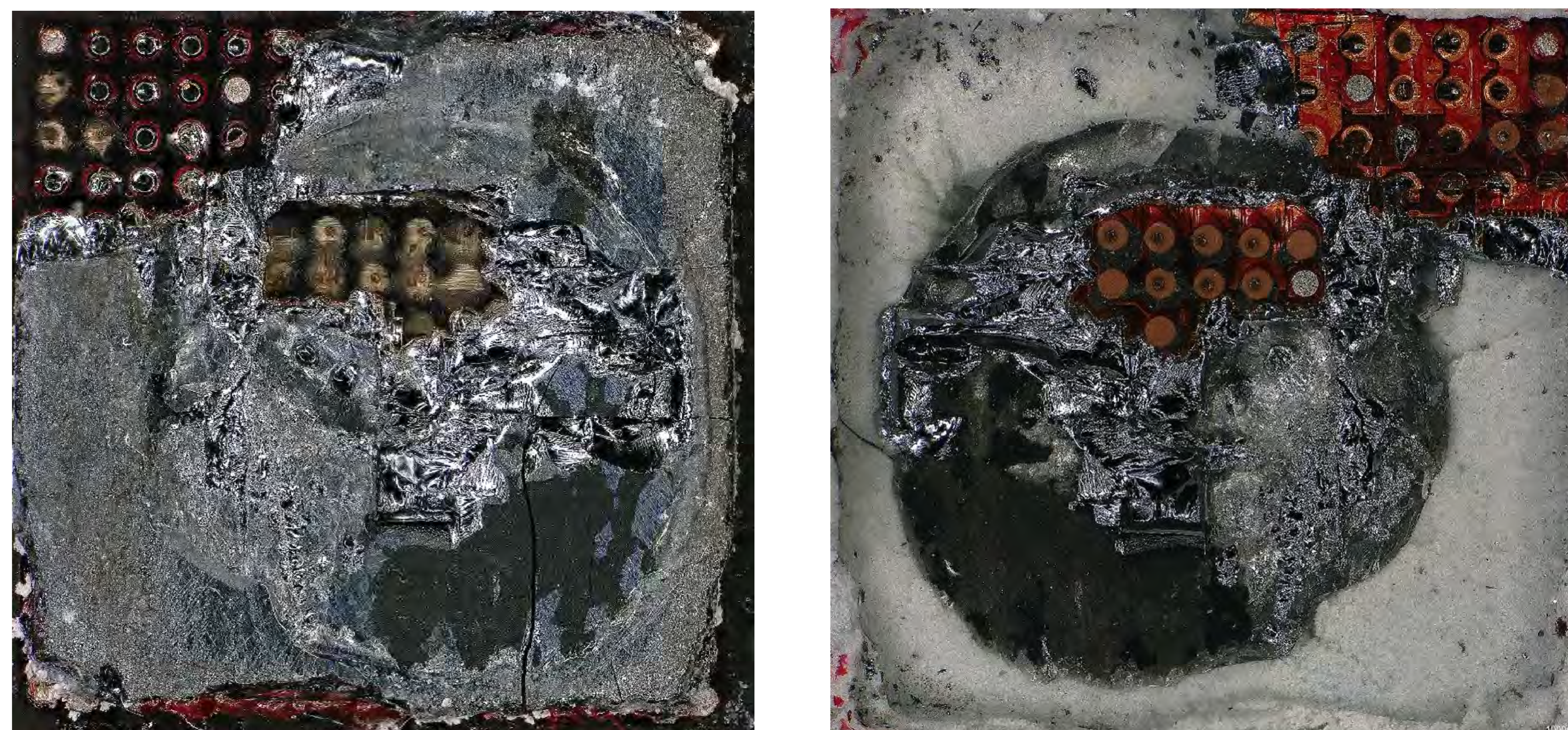


Figure 2: Standard method resulted in the die shattering – making the inspection impossible.

Enhanced Dye and Pull Analysis for CSP Package Types:

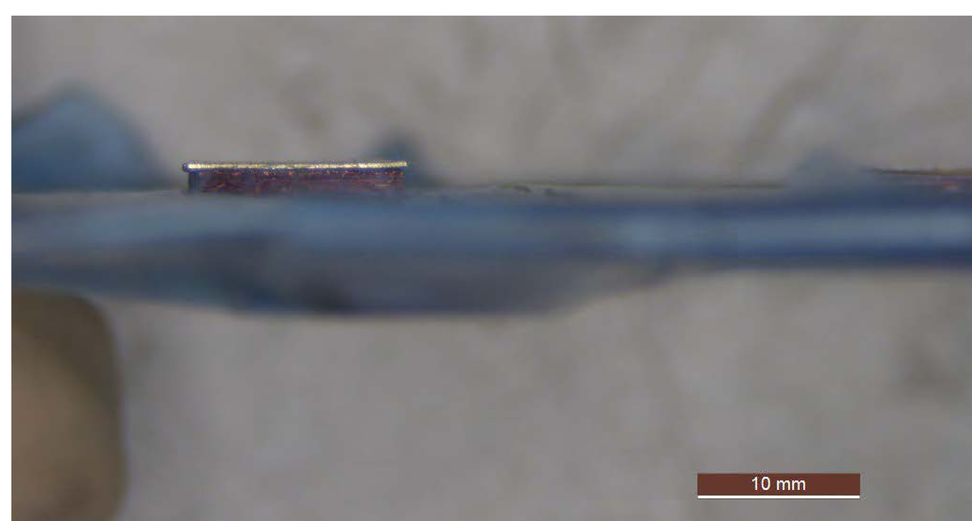


Figure 3: The new process uses a barrier layer placed onto the die & then the cement is attached in preparation for pulling.

PCB **CSP**

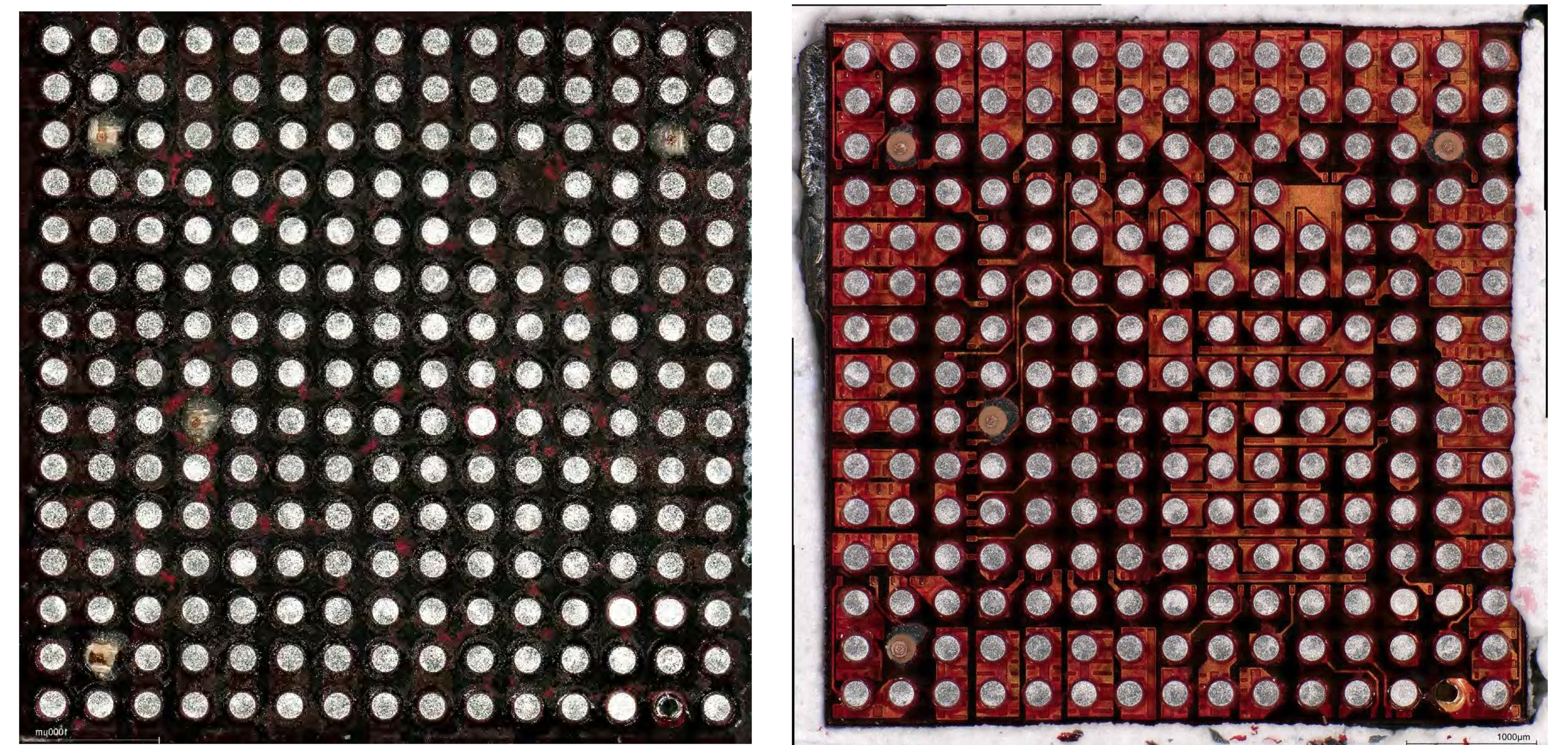


Figure 4: New methodology involved additional CSP prep & optimizing the pulling protocols to accommodate the delicate nature of CSP Si substrates– making the inspection possible.

PCB **CSP**

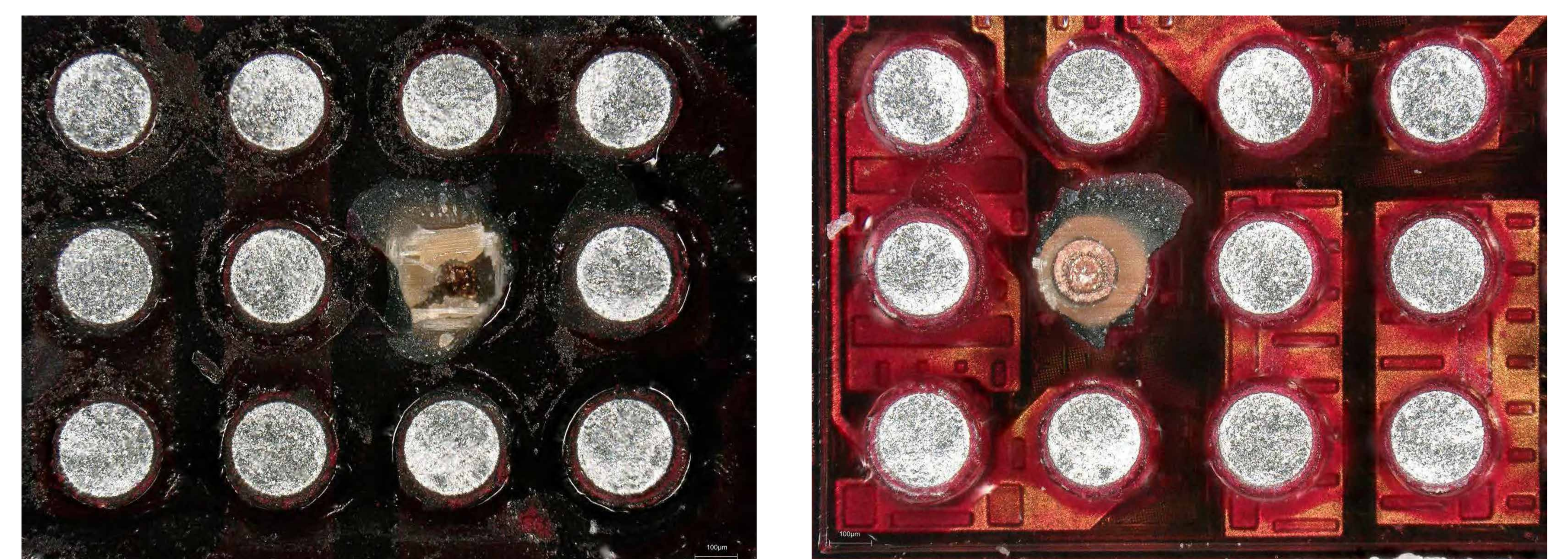


Figure 5: Higher magnification images reveal prying results, with no evidence of red dye ingress at the respective fractured interfaces.

CONCLUSIONS

In this study, we have demonstrated enhancements to the standard Dye and Pull analysis, specifically tailored for CSP's. This advancement enables more reliable solder ball defect detection in CSP's, contributing to improved quality control in semiconductor manufacturing. Future research will concentrate on the further refinement of the pulling technique and investigate its application to additional delicate package types, such as Embedded Wafer Level Ball Grid Arrays (eWLB).