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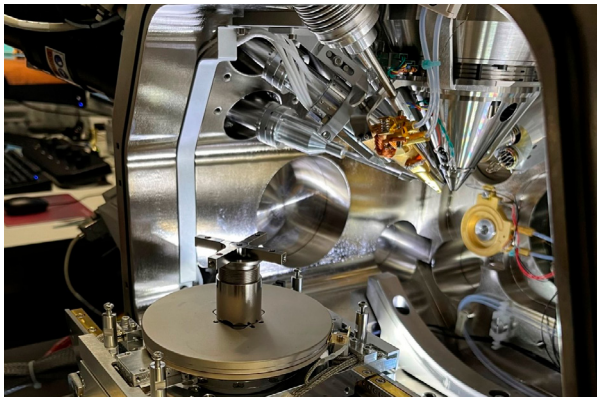
Advancing Semiconductor Failure Analysis: Eurofins EAG's Plasma FIB Delayering

As semiconductor technology evolves, modern devices are designed with enhanced performance and capabilities, featuring more process layers, denser layouts, intricate circuitry, and highly sensitive gate structures—all within shrinking architectures. The growing structural complexity and shrinking feature dimensions of modern devices make identifying and analyzing defects and failures, whether introduced during manufacturing or arising from use, significantly more challenging during failure analysis.

An important physical failure analysis technique for imaging failure mechanisms on a die is deprocessing, also known as delayering. This process involves the controlled removal and exposure of each individual FAB process layer for detailed inspection. However, traditional chemical and mechanical polishing methods used for older, larger semiconductor nodes are no longer viable for the newer generation of technologies, which feature thinner, smaller, and more complex structures.

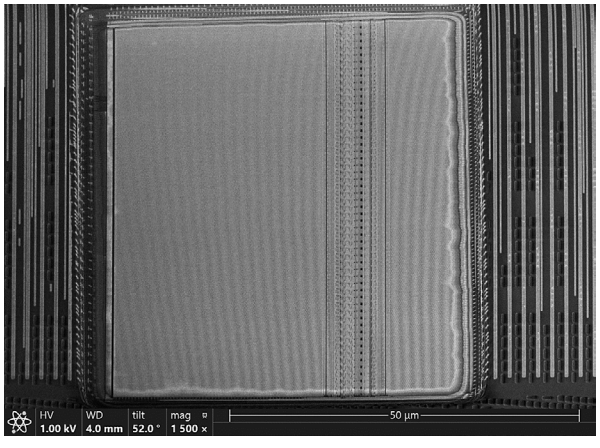


Plasma Focused Ion Beam (PFIB) technology at EAG

At Eurofins EAG Laboratories, we have utilized Plasma Focused Ion Beam (PFIB) to overcome the limitations of traditional deprocessing methods. By leveraging the advanced capabilities of a modern PFIB, we can perform precise, planar removal of individual process layers across large surface areas, even on leading-edge geometry nodes. This approach not only allows our engineers to perform consistent and controlled in-situ inspection of each process layer, but also facilitates other advanced, analytical techniques such as voltage contrast, EBIC/EBAC/EBIRCH, and nanoprobing.

Advantages:

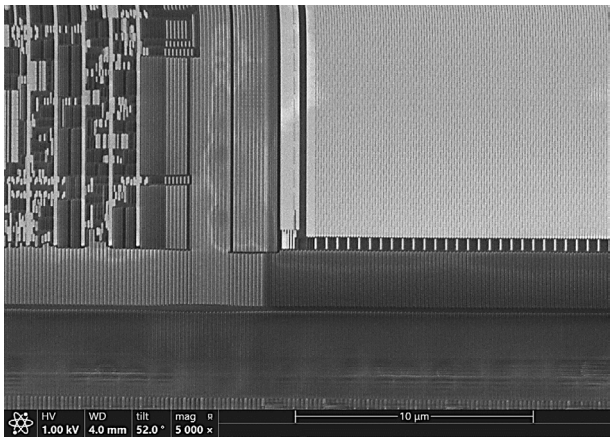
- Large target areas (up to 200 x 200um)
- Precise targeting of single or multiple areas of interest (pursue multiple sites independently, including ones within close proximity to each other)
- Excellent planarity and uniformity in removal of individual process layers
- Minimized and controlled ion beam damage using Xe, not Ga+
- Low Voltage SEM imaging mode to reduce transistor damage (e.g. prep for nanoprobing)



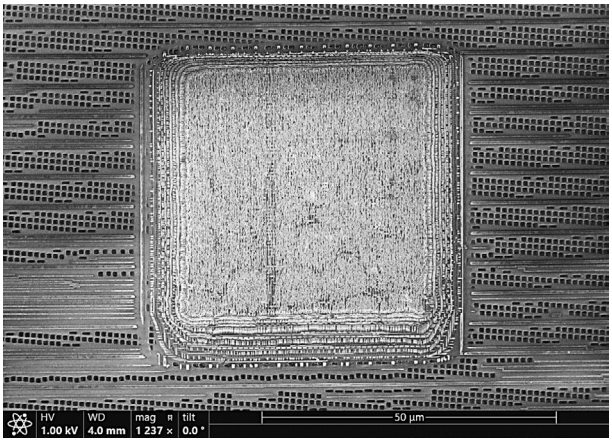
Delayered window with excellent planarity over a large area

Example applications:

- Delayering advanced node device at multiple OBIRCH/Hot spot sites
- Image mask defect issue on low yielding wafer failures
- Identify broken metal line/traces using in-situ voltage contrast analysis during delayering
- Evaluate and validate design/layout and fabrication process
- Enable precision targeting for TEM lamella at lower layer metallization on advanced nodes
- Fault isolation using iterative delayer and nanoprobing at each subsequent process layer



Uniformity of deprocessing on blocks/layout of different densities and features



50um x 50um delayering window with step "staircase" view of the process layers

Contact EAG

EAG provides failure analysis services to help clients achieve high-quality and reliable products. We are dedicated to this mission by offering a one-stop solution for comprehensive engineering services. As a leader in the field, EAG delivers a wide range of services with unparalleled accessibility through our global network of laboratory locations. For more information about our PFIB delayering technique and other offerings, contact EAG today.